UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,931	05/13/2005	Shunpu Li	05-372	3671

20306 7590 10/09/2009

MCDONNELL BOEHNEN HULBERT & BERGHOFF LLP
300 S. WACKER DRIVE
32ND FLOOR
CHICAGO, IL 60606

EXAMINER
BROWN II, DAVID N

ART UNIT	PAPER NUMBER
1791	

MAIL DATE	DELIVERY MODE
10/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,931	LI, SHUNPU	
	Examiner	Art Unit	
	DAVID N. BROWN II	1791	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a final rejection in response to the remarks dated 08/07/2009.

Claim Objections

1. Claims 4 and 8 are objected to because of the following informalities: A claim cannot depend on a cancelled claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3, 5, 7, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0042027 (Chou) in view of US 2006/0035164 (Schaper).

Claim 1:

Chou teaches “Onto the substrate 31 is layered a material 33, which, in the preferred embodiment, is a thin layer of a homopolymer, preferably polymethyl-methacrylate (PMMA). The PMMA was first spun on substrate 31, in this case, a silicon wafer having

a substantially plain flat surface, followed by baking at 80° C. to drive out the solvent. [0035]." Chou also teaches “But, with a mask 35 placed a certain distance above the surface of the PMMA film 33, after the same heat-cool cycle, the initially flat PMMA film 33 became self-assembled into periodic supramolecular pillars 49 shown in FIG. 1. [0037].” Chou teaches the use of two layers. The two layers of Chou include a semi conductive layer and a polymer layer having a pattern introduced by stress. The stress induced by Chou occurs with the semiconductor layer present. Chou does not teach the use of an additional layer such that there are three layers consisting of a substrate, a semiconductive layer, and a patterned polymer layer. Consider Schaper figure 13a. This template comprises a carrier (630) made of a solid material (column 13 lines 12-17), a patterned polymer sheet (610) formed from a PVA polymer, and a metal layer (1302) positioned on the polymer layer. The fact that (1302) is made of metal is taught by Schaper (column14 line 38). Since this object is later used in an imprinting process, it is taken to be a template. Schaper describes the metal layer (1302) as a barrier layer. Schaper teaches “It may also be possible desirable to perform additional processing on the template. The layer on top of the PVA relief provides a convenient coating for the further development, and aids in flexibility since the subsequent processing steps will not interact directly with the delicate PVA material. (column 14 lines 13-18). It would have been obvious to one having ordinary skill in the art at the time of the invention to add an extra metallic layer to the template of Chou motivated by a desire to provide a coating for further development of the template.

Claim 3:

Chou uses PMMA.

Claim 5:

Chou uses silicon as a substrate material.

Claim 7:

Chou teaches “As is described more fully herein, the thin film or surface layer(s) preferably has a thickness in the range of about 1 nm to about 2,000 nm, more preferably about 10 nm to about 1,000 nm, more preferably about 100 nm to about 500 nm and even more preferably about 50 nm to about 250 nm. [0013].”

Claim 27:

The product produced in the process of Chou has undergone an annealing step (baking at 80° C) and a stress-inducing step. Therefore it is taken to be such a template.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou and Schaper in view of US 6,060,556 (DePuydt).

Chou does not teach the use of germanium. Claim 6 of Chou reads “The method of claim 5, wherein the substrate is selected from the group consisting of semiconductors, dielectrics, metals, polymers and combination thereof.” Therefore Chou envisions the use of other semiconductors. Germanium is a known semiconductor material. DePuydt teaches “A semiconductor is typically defined as a material having an electrical resistance greater than a metal, and generally in the range from 10.sup.-2 ohm-cm to 10.sup.9 ohm-cm. In some embodiments, the semiconductor can be selected from the group of germanium, silicon, and combinations thereof. Some particularly preferred combinations of first and second materials 46 and 48 include silicon/aluminum,

germanium/aluminum, germanium/gold. (column 6 lines 13- 19). Thus the substituted semiconductor materials would be expected to perform as equivalents. It would have been obvious to one having ordinary skill in the art at the time of the invention to substitute germanium for silicon motivated by a desire to use another semiconductor.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou and Schaper as applied to claim 1 in view of US 5,772,905 (Chou1).

Chou teaches “U.S. Pat. No. 5,772,905 describes a method and apparatus for performing ultra-fine line lithography wherein a layer of thin film is deposited upon a surface of a substrate and a mold having at least one protruding feature and a recess is pressed into the thin film. [0007] An alternative strategy to those described above is to use a ‘naturally occurring’ or ‘self-assembly’ structure as a template for subsequent parallel fabrication. [0008]” US 5,772,905 (Chou1) teaches " FIG. 4 is a scanning electron micrograph of a perspective view of the strips formed by compressive molding into a PMMA film as shown in FIG. 1C. The strips are 70 nm wide and 200 nm tall, and have a high aspect ratio, a surface roughness less than 3 nm, and corners of nearly a perfect 90 degrees. (Chou1 column 2 line 66- column 3 line 4)

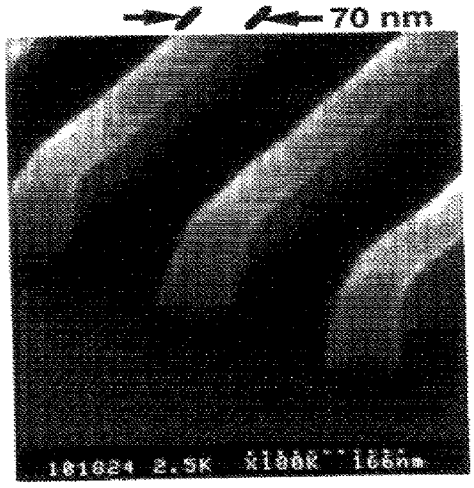

Fig. 4

It would have been obvious to one having ordinary skill in the art at the time of the invention to use this strategy motivated by a desire to use an alternative strategy for fabricating patterns. Also, figure 13B of Chou shows the "Princeton" pattern. Figure 4 of Chou1 shows the parallel groove pattern. Chou teaches in [0064] that "Princeton" was an arbitrary pattern. It would have been obvious to one having ordinary skill in the art to substitute the pattern of Chou1 for the arbitrary "Princeton" pattern of Chou motivated by a desire to change the design.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou and Schaper as applied to claim 1 above, and further in view of US 6,323,108 (Kub).

7. Chou does not teach that the semiconductor layer is 10nm thick. Instead Chou teaches "We found that the materials (for the mask and substrate) and the parameters (e.g., the protrusion height, polymer thickness, polymers molecular weight, gap, etc.) are not very critical to LISC. LISC can be formed over a wide range of these parameters. [0063]" Kub teaches "Ultra-thin (<10 nm) substrates, including silicon-on-insulator (SOI) substrates, are desirable for many technologies including extreme

scaling of MOSFET transistors, dual-gate MOSFETs, quantum wires and dots, and compliant or universal substrates. (column 1 lines 13-17)" Kub also teaches "Ultra-thin semiconductor layers are required for compliant substrates. In structures with a compliant substrate, the ultra-thin semiconductor layer will expand or contract as a heteroepitaxially layer is grown on the surface of the ultra-thin semiconductor layer so that defects, if created, will reside in the ultra-thin semiconductor layer. (column 2 lines 40-45)" Chou teaches using a silicon substrate. It would have been obvious to one having ordinary skill in the art at the time of the invention to use an ultra-thin semiconductor layer upon a substrate motivated by a desire to form nanostructures.

Response to Arguments

8. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID N. BROWN II whose telephone number is (571)270-5497. The examiner can normally be reached on Monday-Thursday 7:30a-5:00p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Del Sole can be reached on (571)-272-1130. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DAVID N. BROWN II/
Examiner, Art Unit 1791

/Joseph S. Del Sole/
Supervisory Patent Examiner, Art Unit 1791